A Novel Sensor Cell Architecture and Sensing Circuit Scheme for Capacitive Fingerprint Sensors

Hiroki Morimura, *Member, IEEE*, Satoshi Shigematsu, *Member, IEEE*, and Katsuyuki Machida, *Member, IEEE*

***Abstract*—Novel capacitive fingerprint sensor techniques are described. We propose a novel sensor cell architecture to obtain high sensitivity, wide output dynamic range, and contrast adjustment. For the architecture, three circuit techniques were developed. A sensing circuit with a differential charge-transfer amplifier enhances sensitivity while it suppresses the influence of the parasitic capacitance of the sensor plate. A wide output dynamic range, which is needed for high-resolution analog-to-digital (A/D) conversion, is achieved by transforming the sensed voltage to a time-variant signal. Finally, the sensing circuit includes an automatic contrast enhancement scheme that uses a variable-threshold Schmitt trigger circuit to distinguish the ridges and valleys of a fingerprint well. The characteristics of a test chip using the 0.5-μm CMOS process show a high sensitivity to less than 80 fF as the detected signal, while the variation of the output signal is suppressed to less than 3% at $\pm$20% variation of the parasitic capacitance. The dynamic range of the time-variant signal is 70 μs, which is wide enough for A/D conversion. The automatic contrast enhancement scheme widens the time-variant signal 100 μs more. A single-chip fingerprint sensor/identifier LSI using the proposed sensing circuit scheme confirms the scheme's effectiveness.**

***Index Terms*—Charge-transfer technique, contrast adjustment, fingerprint sensor, high sensitivity, sensing circuit, sensor cell, time-variant signal, variable threshold, wide dynamic range.**

I. Introduction

CAPACITIVE fingerprint sensors using the CMOS process have been developed for low-power, low-cost, and small-size fingerprint identification systems [1]–[4]. Fig. 1 shows a top view of a fingerprint sensor chip and a schematic cross section of one sensor cell. The chip has a sensor array that captures a fingerprint image when a finger is placed in direct contact with the surface. The array is composed of sensor cells. Each sensor cell consists of a sensor plate and a sensing circuit covered with passivation film. The principle of fingerprint sensing is based on the detection of the capacitance C_f formed between a finger and the sensor plate. The capacitance varies with the pattern of ridges and valleys because they have different distances from the plates. The sensing circuit converts the capacitance to a voltage signal and outputs an analog signal that reflects the fingerprint pattern. However, conventional sensors have some problems to be solved.

Manuscript received August 16, 1999; revised November 29, 1999.

H. Morimura and S. Shigematsu are with the Nippon Telegraph and Telephone Corporation, Lifestyle and Environmental Technology Laboratories, Kanagawa Pref. 243-0198, Japan (e-mail: morimura@aecl.ntt.co.jp).

K. Machida is with the Nippon Telegraph and Telephone Corporation, Telecommunications Energy Laboratories, Kanagawa Pref. 243-0198, Japan.

Publisher Item Identifier S 0018-9200(00)03016-X.

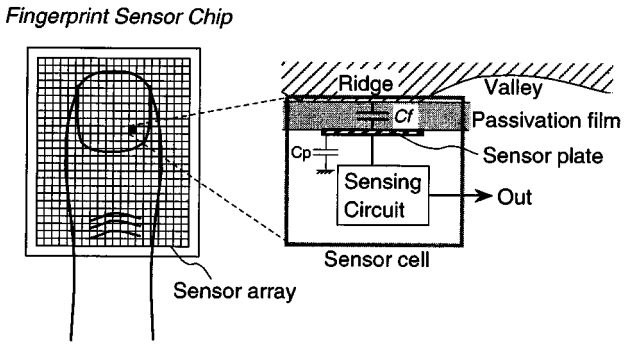

Fig. 1. Capacitive fingerprint sensor.

The main issue for capacitive sensors concerns the sensor plate's parasitic capacitance C_p, which is formed with the interlayer under the sensor plate. The parasitic capacitance is a critical parameter in conventional sensing circuits because C_p is larger than C_f when a standard dielectric film process is used. One conventional technique [2] provides two materials with different dielectric constants and thickness to enlarge the sensed capacitance and reduce the parasitic capacitance. However, for low-cost production, circuit techniques that are independent of the parasitic capacitance should be developed. Another approach is a sensing circuit technique that reduces the influence of the parasitic capacitance by incorporating a shield plate under the sensor plate and controlling the voltage potential of the shield plate [4]. However, the shield plate area is large. Because it is made of the second metal layer in the sensor cell, implementation of high-density circuits is prevented. For this problem too, a sensing circuit scheme that is independent of the parasitic capacitance is essentially needed.

Another issue is the need for a wide output dynamic range. To obtain a clear fingerprint image, the analog signals from the sensor should be converted to high-resolution digital signals. However, the output dynamic range of conventional sensing circuits is not wide enough because it is restricted in a linear region of the analog amplifier [1] or the small sensing signal is directly compared with the reference voltage $V_{\rm ref}$ [2]–[4]. Hence, the resolution analog-to-digital (A/D) conversion has been limited, and this degrades a captured fingerprint image.

A third issue is contrast adjustment. Contrast adjustment is effective for distinguishing ridges and valleys, but, in conventional fingerprint sensors, it is performed by software in external equipment. For single-chip implementation of the sensor and fingerprint identification system, the contrast adjustment must be implemented in the chip. A local contrast adjustment technique has been implemented in a sensor chip [5]. However, this

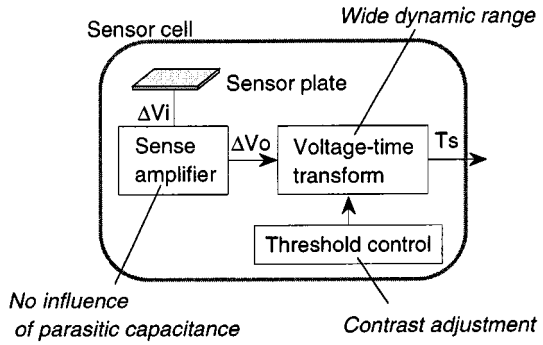

Fig. 2. Sensor cell architecture.

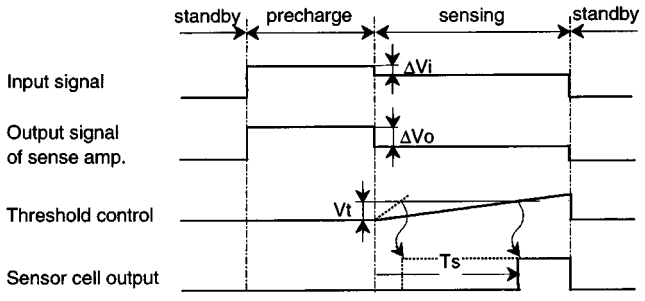

Fig. 3. Sensing operation.

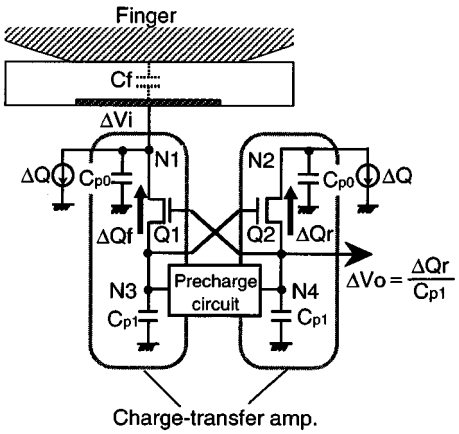

Fig. 4. Sensing circuit with charge-transfer amplifier.

is used to adjust the reference voltage for image binarization, not for contrast adjustment of the whole image. Another problem with this approach is that it reduces the effective sensing signal voltage, which is the difference between the sensed voltage and the reference voltage.

This paper describes novel capacitive fingerprint sensor techniques for fingerprint sensors. First, a new sensor cell architecture is proposed in Section II. Section III describes sensing circuit techniques for high sensitivity, wide output dynamic range, and contrast adjustment. The characteristics of a test chip fabricated with the 0.5-μm CMOS process and application to a single-chip fingerprint sensor/identifier LSI (FIL) [6] are presented in Section V.

II. Sensor Cell Architecture

The proposed sensor cell architecture is shown in Fig. 2. Each sensor cell is composed of a sensor plate, a sense amplifier, and a voltage-time transform unit, and incorporates a threshold control scheme. The sense amplifier eliminates the influence of the parasitic capacitance of the sensor plate. The voltage-time transform unit widens the output dynamic range, and the threshold control enhances the signal contrast. The circuit techniques used to create this architecture are described in the next section.

The sensing operation is shown in Fig. 3. First, input signal ΔV_i, which is correlative to the capacitance associated with the sensor plate, is generated after the precharge operation. ΔV_i is sensed and amplified to ΔV_o without dependence on the parasitic capacitance. After that, ΔV_o is transformed to time-variant signal T_s to enlarge the output dynamic range. Finally, T_s is varied by controlling threshold voltage V_t in the voltage-time transform circuit to enhance the contrast between signals at ridges and valleys.

The proposed architecture enables us to get high-sensitivity, wide output dynamic-range and contrast adjustment.

III. Sensing Circuit Scheme

A. High-Sensitivity Sensing Scheme on Large Parasitic Capacitance

The capacitive fingerprint sensing scheme with the charge-transfer technique is shown in Fig. 4. Input signal ΔV_i is generated by discharging ΔQ from capacitance C_f formed between the sensor plate and finger surface. The sensor plate has parasitic capacitance C_{p0} in a practical device. Accordingly, ΔV_i is expressed as

$$\Delta V_i = \Delta Q/(C_f + C_{p0}). \tag{1}$$

This means that detecting ΔV_i becomes difficult because its value is reduced when C_{p0} becomes larger than C_f. The sensing circuit with the charge-transfer technique can enhance the sensitivity even if the parasitic capacitance of the sensor plate is large. High sensitivity is achieved because only the amount of transferred charge is sensed. The sensing circuit features the cross-coupling of differential charge-transfer amplifiers Q_1 and Q_2.

Fig. 5(a) shows the whole waveform of the sensing circuit. After the precharge operation, the sensing circuit has three operation modes: transient region I ($t_0 \le t \le t_1$), transient region II ($t_1 \le t \le t_2$), and dc region ($t_2 \le t \le t_3$). These operations are qualitatively explained as follows.

1) Precharge Operation: N_1 and N_2 are precharged at $V_{\rm DD} - V_{\rm th}$ through Q_1 and Q_2. $V_{\rm DD}$ is the supply voltage and $V_{\rm th}$ is the threshold voltage of Q_1 and Q_2. After precharge, the sensing operation starts.

2) Sensing Operation—Transient Region I: When ΔQ is discharged from N_1 and N_2 at t_0, the sensing operation starts and input signal ΔV_i is generated. After that, charges ΔQ_f and ΔQ_r begin to be transferred from N_3 and N_4 to N_1 and N_2 through Q_1 and Q_2. ΔQ_f and ΔQ_r are not the same because the voltage of N_1 is different from that of N_2 due to C_f. This causes a voltage difference between N_3 and N_4. The voltage

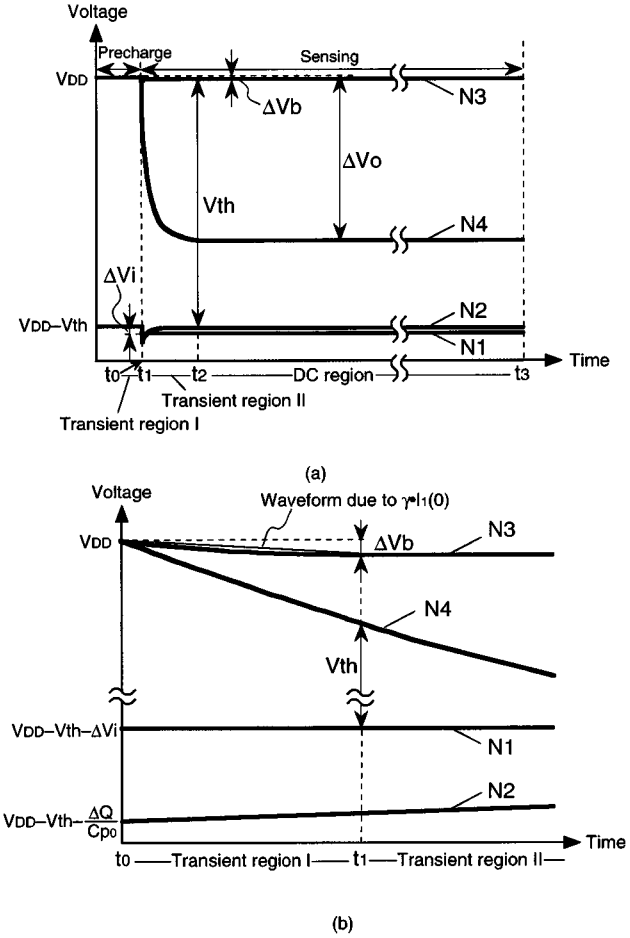

Fig. 5. Waveform of sensing circuit: (a) in the whole operation and (b) around transient region I.

change of N_3 stops at t_1 because the gate-source voltage $V_{\rm GS}$ of Q_1 becomes $V_{\rm th}$, and Q_1 is cut off. The voltage change ΔV_b of N_3 is fixed as $\Delta Q_f/C_{p1}$, where C_{p1} is the capacitance of N_3. After that, the operation mode moves to transient region II.

3) Sensing Operation—Transient Region II: ΔV_b, fixed in transient region I, acts as bias voltage for the gate node of Q_2 in transient region II. This controls the amount of ΔQ_r. The voltage change of N_4 continues until t_2. The voltage change of N_4 stops at t_2 because $V_{\rm GS}$ of Q_2 becomes $V_{\rm th}$, and Q_2 is cut off. The final voltage change ΔV_o of N_4 becomes $\Delta Q_r/C_{p1}$ at t_2. The mode then moves to the dc region.

4) Sensing Operation—DC Region: The dc region is maintained from t_2 to t_3. In this operation, the voltages of N_1, N_2, N_3, and N_4 are not changed, and voltage-time transformation is performed as explained in Section III-B. The sensing operation is completed at t_3.

Consequently, the sensing operation is as follows. The sensing operation starts at t_0. The voltage change of N_3 and N_4 stops at t_1 and t_2, respectively. The sensing operation is almost completely performed in the dc region until t_3. C_{p1} becomes small in the practical layout design, so the voltage changes of N_3 and N_4 are enhanced. The differential scheme also reduces the variation of ΔV_o due to the noise on the supply voltage and the subthreshold leakage current of Q_1 and Q_2.

In the sensing circuit, these expressions consist of:

$$dV_1(t)/dt = I_1(t)/(C_f + C_{p0}) \tag{2}$$

$$dV_2(t)/dt = I_2(t)/C_{p0} \tag{3}$$

$$dV_3(t)/dt = -I_1(t)/C_{p1} \tag{4}$$

$$dV_4(t)/dt = -I_2(t)/C_{p1} \tag{5}$$

$$I_1(t) = K \bullet (V_4(t) - V_1(t) - V_{\rm th})^{\alpha} \tag{6}$$

$$I_2(t) = K \bullet (V_3(t) - V_2(t) - V_{\rm th})^{\alpha} \tag{7}$$

$$V_1(t_0) = V_{\rm DD} - V_{\rm th} - \Delta Q/(C_f + C_{p0}) \tag{8}$$

$$V_2(t_0) = V_{\rm DD} - V_{\rm th} - \Delta Q/C_{p0} \tag{9}$$

$$V_3(t_0) = V_{\rm DD} \tag{10}$$

$$V_4(t_0) = V_{\rm DD} \tag{11}$$

where $V_1(t)$, $V_2(t)$, $V_3(t)$, and $V_4(t)$ are the voltages of N_1, N_2, N_3, and N_4, respectively. $I_1(t)$ and $I_2(t)$ obey the α-power law of the saturation current of Q_1 and Q_2. K is a constant. The characteristics of the sensing circuit are estimated analytically, as follows.

Fig. 5(b) shows the waveform of the sensing circuit around transient region I. When the voltage change of N_4, $\Delta V_4(t) = V_4(t_0) - V_4(t)$, becomes almost equal to ΔV_i at t_1, the voltage change of N_3 stops because $V_{\rm GS}$ of Q_1 is equal to $V_{\rm th}$. The voltage of N_1 is assumed to be constant from t_0 to t_1 because the voltage change of N_3 is small and C_{p0} is much larger than C_{p1}. The current $I_2(t)$ between t_0 and t_1 is almost constant and equal to $I_2(t_0)$ because of $t_1 \ll t_2$. For ease of explanation, t_0 is equal to zero in this discussion. Then, $\Delta V_4(t_1)$ is approximated from (5) as

$$\begin{aligned}\Delta V_4(t_1) &= V_4(t_0) - V_4(t_1) \\ &= \int_{t_0}^{t_1} I_2(t)\,dt/C_{p1} \\ &\approx I_2(0) \bullet t_1/C_{p1}.\end{aligned} \tag{12}$$

$\Delta V_4(t_1)$ is almost equal to ΔV_i, and from (1) and (12)

$$I_2(0) \bullet t_1/C_{p1} \approx \Delta Q/(C_f + C_{p0}). \tag{13}$$

ΔQ_f is expressed by introducing the weight parameter γ such that

$$\begin{aligned}\Delta Q_f &= \int_{t_0}^{t_1} I_1(t)\,dt \\ &= \gamma \bullet I_1(0) \bullet t_1 \qquad (0 < \gamma < 1).\end{aligned} \tag{14}$$

The condition of γ is obtained because ΔQ_f does not become zero and $I_1(t)$ becomes smaller than $I_1(0)$ at $t > 0$. The waveform of N_3 due to this assumption of (14) is also plotted in Fig. 5(b). This waveform shows that the condition $0 < \gamma < 1$ is appropriate. From (14)

$$\begin{aligned}\Delta V_b &= \Delta Q_f / C_{p1} \\ &= \gamma \bullet I_1(0) \bullet t_1 / C_{p1}. \end{aligned} \tag{15}$$

From (13) and (15)

$$\Delta V_b = \gamma \bullet I_1(0)/I_2(0) \bullet \Delta Q/(C_f + C_{p0}). \tag{16}$$

When the difference of the voltages of N_3 and N_2 becomes $V_{\rm th}$ at t_2, as shown in Fig. 5(a), the voltage change of N_4 stops because Q_2 is cut off. Then $V_2(t)$ at t_2 is expressed as

$$V_2(t_2) = V_{\rm DD} - \Delta V_b - V_{\rm th}. \tag{17}$$

From (3), (9), (16), and (17)

$$\begin{aligned}\Delta Q_r &= \int_{t_0}^{t_2} I_2(t)\, dt \\ &= C_{p0}(V_2(t_2) - V_2(t_0)) \\ &= \Delta Q - C_{p0} \bullet \Delta V_b \\ &= \Delta Q\{1 - \gamma \bullet I_1(0)/I_2(0) \bullet C_{p0}/(C_f + C_{p0})\}. \end{aligned} \tag{18}$$

From (6) to (11)

$$I_1(0) = K \bullet \{\Delta Q/(C_f + C_{p0})\}^{\alpha} \tag{19}$$

and

$$I_2(0) = K \bullet (\Delta Q/C_{p0})^{\alpha}. \tag{20}$$

Therefore, ΔV_o is obtained from (18)–(20) as

$$\begin{aligned}\Delta V_o &= \Delta Q_r / C_{p1} \\ &= \Delta Q/C_{p1} \bullet \{1 - \gamma/(1 + C_f/C_{p0})^{\alpha+1}\} \\ &\quad (0 < \Delta Q/C_{p1} \le V_{\rm th}). \end{aligned} \tag{21}$$

The maximum output voltage change of the charge-transfer amplifier Q_2 is $V_{\rm th}$. Hence, $\Delta Q/C_{p1}$ must be designed so that $0 < \Delta Q/C_{p1} \le V_{\rm th}$.

Fig. 6 shows the relationship between C_f/C_{p0} and ΔV_o, which is normalized by $\Delta Q/C_{p1}$, obtained from (21) for α of 1.5 and γ of 0.5. The result of numeric calculation by using (2)–(11) is also plotted. The figure shows that (21) explains the essential operation of the sensing circuit and is available to design the capacitive fingerprint sensor. Below 0.1 of C_f/C_{p0}, the results of (21) and the numeric calculation do not match well. This is because the approximation in (12) is not suitable when $C_f \ll C_{p0}$, i.e., when t_2 is close to t_1. However, (21) becomes useful also in the case of $C_f \ll C_{p0}$ by treating γ as a variable parameter. This is because γ is dependent on C_f and can include the treatment of the integration of $I_2(t)$ in (12) as in (14). In this consideration, γ increases when C_f becomes small, and ΔV_o is close to $\Delta Q/C_{p1} \bullet (1 - \gamma)$. When C_f is zero, 0.91 of γ is obtained from the numeric calculation.

In Fig. 6, the change of the normalized ΔV_o is large when C_f/C_{p0} is less than one. This means the sensitivity of the sensing circuit is enhanced even though the parasitic capacitance C_{p0} is larger than the sensed capacitance C_f. Therefore, the sensing circuit with a differential charge-transfer amplifier has high sensitivity on the large parasitic capacitance of the sensor plate.

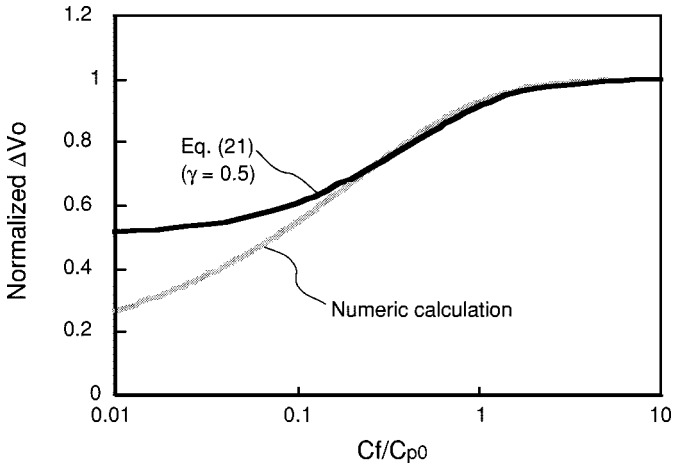

Fig. 6. Estimated relationship between C_f/C_{p0} and ΔV_o.

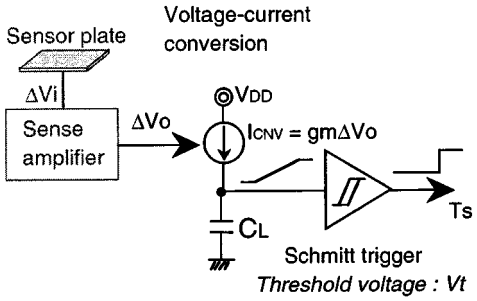

Fig. 7. Voltage-time transform circuit.

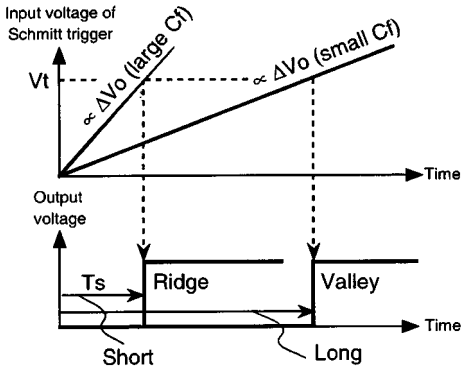

Fig. 8. Waveform of voltage-time transform circuit.

B. Dynamic-Range Widening Method

The dynamic range of ΔV_o is equal to or smaller than the threshold voltage of Q_2, so we make the dynamic range wide by transforming ΔV_o to time-variant signal T_s. The voltage-time transform circuit is shown in Fig. 7. It is composed of a current source, a load capacitor C_L, and a Schmitt trigger circuit as a threshold circuit. Fig. 8 shows the operation of the voltage-time transform circuit. First, ΔV_o is converted to current $I_{\rm CNV}$ $(=g_m \Delta V_o)$, which charges C_L. The transconductance of the

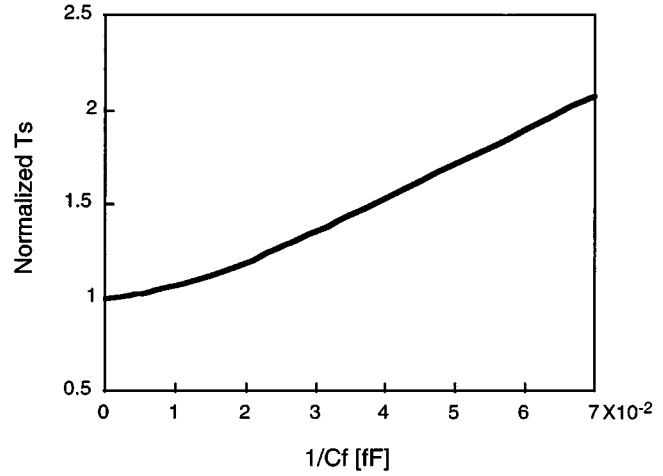

Fig. 9. Estimated relationship between $1/C_f$ and T_s.

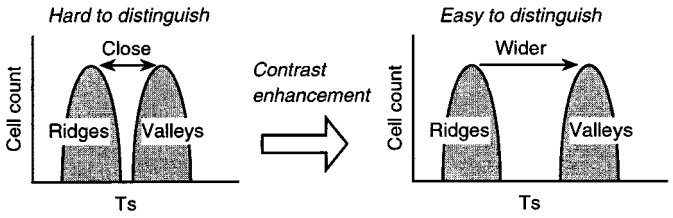

Fig. 10. Concept of contrast enhancement scheme.

ideal current source is expressed as g_m. When the charged voltage of C_L exceeds threshold voltage V_t, the Schmitt trigger circuit outputs high-level signal T_s, which is time variant. T_s is expressed as

$$T_s = C_L \bullet V_t / I_{\mathrm{CNV}} \tag{22}$$

$$= C_L \bullet V_t / g_m \Delta V_o. \tag{23}$$

For large detected capacitance, the input signal of the Schmitt trigger has a steep slope due to large ΔV_o, as shown in Fig. 6, so T_s is short. For small C_f, the slope is gradual due to small ΔV_o, and T_s becomes longer. Because the slope of the input signal of the threshold circuit is gradual, the Schmitt trigger is used to prevent miss-operation due to voltage fluctuation caused by noise.

In practice, a PMOSFET that is operated in the subthreshold region is used for the current source (Q_5 in Fig. 14) because the subthreshold leakage current is small, and it enlarges T_s as shown in (22). So I_{CNV} is expressed as

$$\begin{aligned} I_{\mathrm{CNV}} &= I_{\mathrm{SUB}} \exp((V_{\mathrm{GS}} - V_{\mathrm{th}})/(n \bullet kT/q)) \\ &= I_{\mathrm{SUB}} \exp((\Delta V_o - V_{\mathrm{th}})/(n \bullet kT/q)) \end{aligned} \tag{24}$$

where

- k Boltzmann's constant;
- T temperature;
- q electronic charge;
- n parameter of the subthreshold swing.

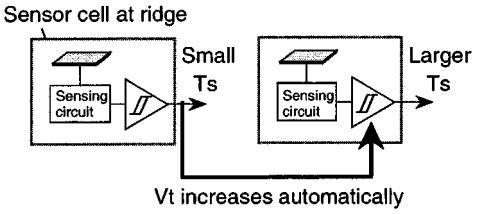

Fig. 11. Principle of automatic contrast enhancement.

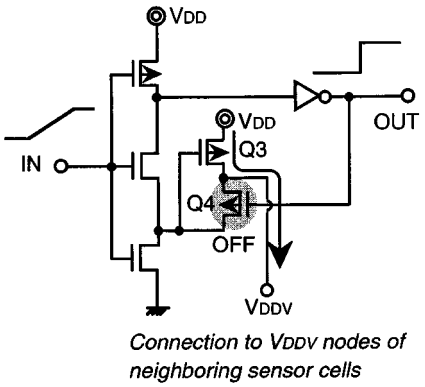

Fig. 12. Variable-threshold Schmitt trigger.

I_{SUB} is the leakage current when V_{GS} is equal to V_{th}. From (21), (22), and (24)

$$\begin{aligned} T_s &= C_L \bullet V_t / I_{\mathrm{SUB}} \bullet \exp\{-\{(\Delta V_o - V_{\mathrm{th}})/(n \bullet kT/q)\}\} \\ &= T_0 \bullet \exp\{-\Delta Q / C_{p1} \bullet \{1 - \gamma/(1 + C_f/C_{p0})^{\alpha+1}\}/ \\ &\quad (n \bullet kT/q)\} \end{aligned} \tag{25}$$

and

$$T_0 = C_L \bullet V_t / I_{\mathrm{SUB}} \bullet \exp\{V_{\mathrm{th}}/(n \bullet kT/q)\}. \tag{26}$$

In practice, the voltage-time transform circuit is activated at t_0, but the (25) is available because t_3 is much larger than t_2, as shown in Fig. 5(a). Fig. 9 shows the relationship between $1/C_f$ and T_s, which is normalized by T_0, as estimated from (25) with $\Delta Q/C_{p1} = 0.2$ V, $C_{p0} = 30$ fF, and $n = 2$. From the results in Fig. 6, we use a parameter γ value of 0.5, because C_f/C_{p0} is larger than 0.1 in this estimation.

T_s is approximated to be inversely proportional to C_f in this region. This means that T_s is proportional to the distance from the sensor plate to the finger surface. Therefore, T_s is short for large C_f (at the ridge) and long for small C_f (at the valley), which yields a wide dynamic range. In this circuit, the output dynamic range is wide enough to obtain an accurate fingerprint image with an A/D converter.

C. Automatic Contrast Enhancement Scheme

C_f is presumed to be localized near two values in response to the ridges and valleys in a fingerprint. Fig. 10 shows the distribution of sensor cell count against T_s responding to ridges and valleys. To obtain a high-contrast fingerprint image, the output signals at ridges and valleys should be distinguished well. When the values of these signals are close, it is hard to distinguish between ridges and valleys. However, if the difference between

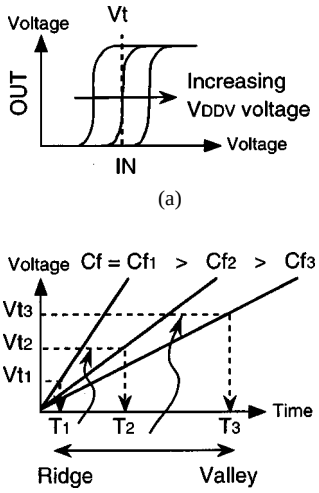

Fig. 13. Threshold control operation. (a) Varying threshold voltage V_t by V_{DDV} voltage. (b) Increasing T_s due to increased V_t.

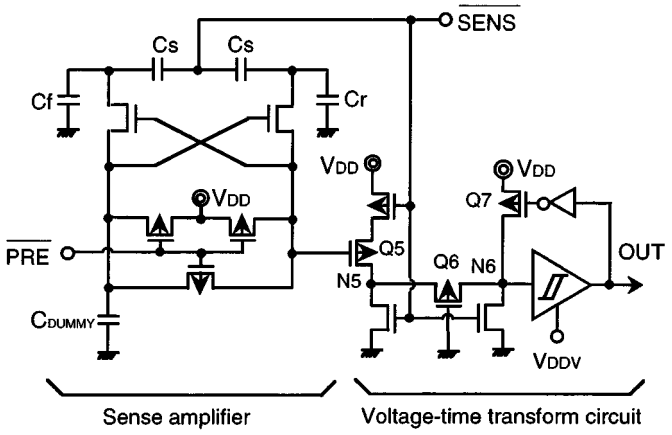

Fig. 14. Sensing circuit configuration.

the values is widened, the ridges and valleys can be easily distinguished. The basic idea of contrast enhancement is that the contrast between ridges and valleys is strengthened by making the T_s of valleys larger.

Fig. 11 shows the principle of the automatic contrast enhancement scheme. The key point is that any sensor cell that has done sensing can assist other cells that are still working. That is, a sensor cell that has sensed a ridge outputs a feedback signal to sensor cells working on valleys. In practical design, the output signal at a ridge increases the V_t of the Schmitt trigger, which, from (26), automatically makes T_s larger. The variable-threshold Schmitt trigger circuit is shown in Fig. 12. V_t becomes large when the voltage of the V_{DDV} node increases, as shown in Fig. 13(a). This node is connected to other V_{DDV} nodes of neighboring sensor cells. When a sensor cell outputs a high-level signal, the current from Q_3 is supplied to other sensor cells because Q_4 is cut off. This causes the voltage of the V_{DDV} node to become high and enlarges the V_t of the sensor cells that are still sensing (outputting a low-level signal).

Fig. 13(b) shows the threshold control operation. T_1 is output first, then this raises V_{t_1} to V_{t_2} of other Schmitt trigger circuits. After that, T_2 is enlarged and output by increased V_{t_2}.

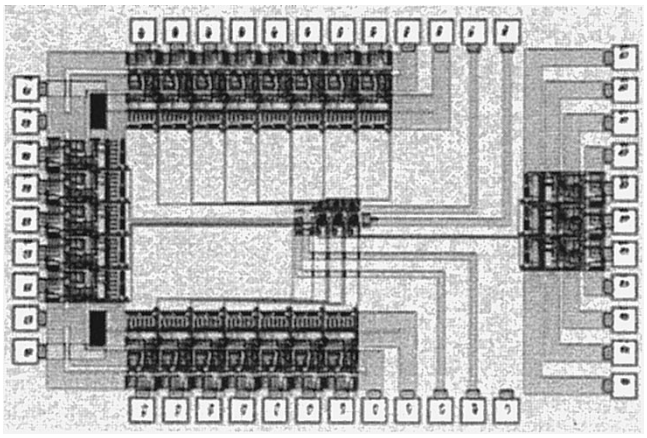

Fig. 15. Test chip.

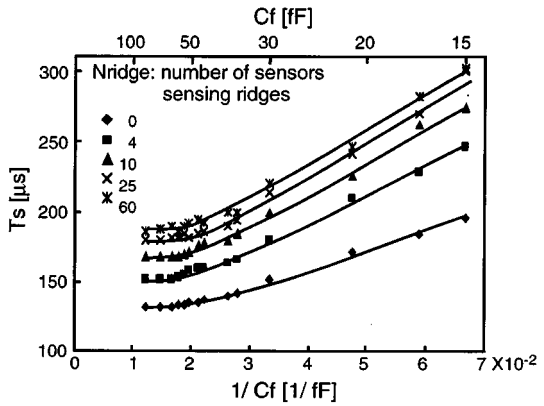

Fig. 16. Relationship between C_f and T_s.

This raises V_{t_2} to V_{t_3}, and this action is repeated automatically. Therefore, the T_s of sensor cells at a valley (small C_f) is enlarged more than that of cells at a ridge (large C_f). Consequently, the contrast of the signals at the ridge and valley is enhanced automatically.

IV. Experimental Results

A. Characteristics of the Sensing Circuit

The characteristics of the sensing circuit were evaluated using a test chip fabricated with the 0.5-μm CMOS process. Fig. 14 shows the sensing circuit configuration based on the proposed scheme. Sensing begins when the C_s capacitors discharge by lowering the sense-enable signal. Capacitance C_s is used to generate the precise amount of ΔQ with simple control. C_f is added to imitate the capacitance associated with the sensor plate. C_r is used for offset adjustment. PMOSFET Q_5 is used for voltage–current conversion. C_{DUMMY}, which is made from the dummy circuit of Q_5, compensates the parasitic capacitance of differential nodes. Q_6 and Q_7 are added to reduce the power dissipation of the Schmitt trigger. The voltage of N_6 is GND until the voltage of N_5 exceeds the threshold voltage of Q_6, and is set to the supply voltage when OUT is changed to "high." This reduces the total sink current of the Schmitt trigger.

The test chip is shown in Fig. 15. The chip size is 2 mm $\times$ 3 mm. C_f, C_r, and C_s are made of MOS capacitances. C_f and C_r are designed to be adjustable at measurement. This

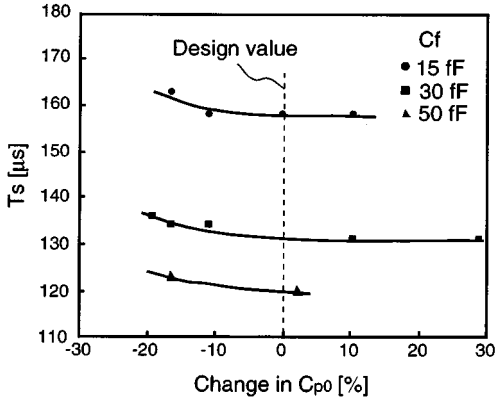

Fig. 17. Dependence of T_s on C_{p0} variation.

chip can emulate the automatic contrast enhancement scheme. Fig. 16 shows the relationship between C_f and T_s. The horizontal axis is $1/C_f$ and the parameter is $N_{\rm ridge}$, which is the number of sensors sensing ridges (to be exact, output "high"). T_s becomes large as $1/C_f$ increases (C_f decreases). This is in accordance with Fig. 9. This confirms that the estimation model introduced for the parameter γ of the sensing circuit is adequate, and (21), (25), and (26) are very useful for the capacitive fingerprint sensor design.

At $N_{\rm ridge} = 0$, which means that there is no threshold control, T_s changes from 130 to 200 μs when C_f is 80 and 15 fF. A high sensitivity with a wide output dynamic range is obtained. Moreover, T_s becomes larger overall as $N_{\rm ridge}$ increases owing to the automatic contrast enhancement scheme. When C_f at a valley is localized at around 15 fF, T_s increases from 200 to 300 μs as $N_{\rm ridge}$ goes from 0 to 60. This means that the contrast is enhanced by enlarging the difference between T_s at a ridge and T_s at a valley.

Fig. 17 shows the dependence of T_s on the percent change in the parasitic capacitance C_{p0} of the sensor plate. The variation of T_s is suppressed to less than 3% at $\pm$20% variation of C_{p0}. This shows that the sensing circuit is hardly influenced by the parasitic capacitance in practical use. From (25), T_s should be shorter when C_{p0} decreases, but this is not observed. This is explained as follows. When C_{p0} reduces, the effective ΔQ also reduces because ΔQ is generated by C_s. That is, ΔQ is positive dependent on C_{p0} in the designed circuit as shown in Fig. 14. From (25), this increases T_s. Thus, generating ΔQ by C_s compensates for the dependence of T_s on C_{p0}. As a result, the almost flat characteristic of T_s on C_{p0} is obtained.

These characteristics of the test chip ensure that the performance of the sensing circuit is high enough for fingerprint sensors.

B. Application to Fingerprint Sensor/Identifier LSI

The sensing circuit scheme has been applied to a single-chip fingerprint sensor/identifier LSI (FIL) [6]. A microphotograph of the FIL and the layout pattern of the sensing circuit in one pixel are shown in Fig. 18. The size of the FIL is 15$\times$ 15 mm^2. The FIL is composed of a 124 $\times$ 166 pixel array, a controller, and a small program memory. Each pixel contains a sensor cell and an identifier cell. The size of one pixel is 81.6 $\times$ 81.6 μm^2.

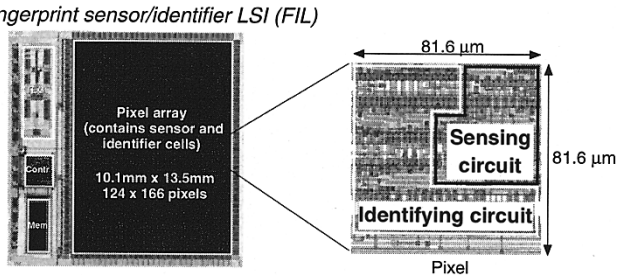

Fig. 18. Sensing circuit pattern of fingerprint sensor/identifier LSI (FIL).

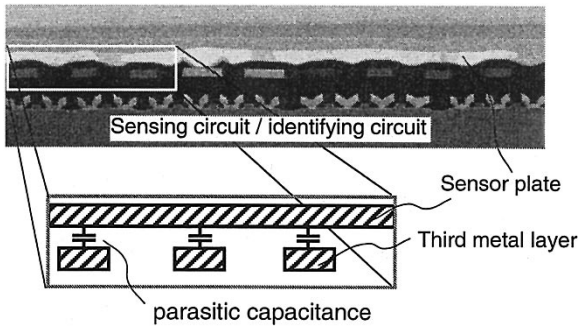

Fig. 19. FIB cross-section of pixel array.

Fig. 20. Captured fingerprint image (124 $\times$ 166).

The $V_{\rm DDV}$ node in the sensing circuit is connected among the 124 horizontal cells. A focused ion beam (FIB) cross-section of the pixel array is shown in Fig. 19. The sensing circuit is accommodated below a sensor plate without an area penalty. The plate has a large parasitic capacitance with respect to the interlayer. However, the sensing circuit is not affected by it at all, as described in Section IV-A. The fingerprint bitmap image obtained by the FIL is shown in Fig. 20. C_f is sensed and binarized in each cell, and the fingerprint image is captured as bitmap data. Though there may be an adverse effect on the sensitivity from the large parasitic capacitance predicted from Fig. 19, an accurate high-contrast image was obtained. Therefore, it can be concluded that the proposed sensing scheme is very useful for integrated fingerprint sensors.

V. Conclusion

New capacitive fingerprint sensor techniques are described. A new sensor cell architecture, which obtains high sensitivity, wide output dynamic range, and contrast adjustment, has been proposed. To create the architecture, three circuit techniques were developed.

A sensing circuit with a differential charge-transfer amplifier, which enhances the sensitivity even though the parasitic capacitance of the sensor plate is large, detects slight capacitance differences according to the ridges and valleys in a fingerprint. For high-resolution A/D conversion, the dynamic range of the sensor output is widened by transforming sensed signal ΔV_o to time-variant signal T_s using a voltage–current conversion circuit and a Schmitt trigger circuit. Finally, an automatic contrast enhancement scheme adjusts the threshold voltage of Schmitt trigger using the output signal of each sensor cell.

The characteristics of the sensing circuit were estimated analytically using a model that introduced parameter γ. A comparison of the analytical estimation with the numeric calculation and experimental measurements confirmed that the estimation is adequate and the derived equations are very useful for capacitive fingerprint sensor design.

Experiments using a test chip fabricated with the 0.5-μm CMOS process to evaluate the characteristics of the sensing circuit confirmed a high sensitivity to less than 80 fF of C_f with a wide output dynamic range of 70 μs. The T_s variation is suppressed to less than 3% at $\pm$20% variation of C_{p0}. Moreover, the automatic contrast enhancement scheme enlarges T_s at 15 fF of C_f 100 μs more. An accurate high-contrast fingerprint image was obtained by applying the sensing scheme in a single-chip fingerprint sensor/identifier LSI, and the effectiveness of the proposed sensing circuit scheme was confirmed.

Acknowledgment

The authors would like to thank K. Takeya, R. Kasai, J. Yamada, S. Konaka, H. Kyuragi, and T. Wakimoto for their encouragement and support. The authors also would like to thank Y. Tanabe, K. Kudou, and M. Yano for the fabrication of the chips; Y. Komine for FIB measurement; and N. Sato for the numeric calculation of the sensing circuit.

References

[1] M. Tartagni and R. Guerrieri, "A fingerprint sensor based on the feedback capacitive sensing scheme," *IEEE J. Solid-State Circuits*, vol. 33, pp. 133–142, Jan. 1998.

[2] D. Inglis, L. Manchanda, R. Comizzoli, A. Dickinson, E. Martin, S. Mendis, P. Silverman, G. Weber, B. Ackland, and L. O'Gorman, "A robust, 1.8V 250μW direct-contact 500dpi fingerprint sensor," in *ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 284–285.

[3] J. Lee, D. Min, J. Kim, and W. Kim, "A 600-dpi capacitive fingerprint sensor chip and image-synthesis technique," *IEEE J. Solid-State Circuits*, vol. 34, pp. 469–475, Apr. 1999.

[4] S. Jung, R. Thewes, T. Scheiter, K. Goser, and W. Weber, "A low-power and high-performance CMOS fingerprint sensing and encoding architecture," *IEEE J. Solid-State Circuits*, vol. 34, pp. 978–984, July 1999.

[5] ——, "CMOS fingerprint sensor with automatic local contrast adjustment and pixel parallel encoding logic," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1999, pp. 161–164.

[6] S. Shigematsu, H. Morimura, Y. Tanabe, and K. Machida, "A 15 $\times$ 15mm^{2}single-chip fingerprint sensor and identifier using pixel parallel processing," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 138–139.

Hiroki Morimura (M'96) was born in Saitama, Japan, on January 9, 1968. He received the B.E. degree in physical electronics and the M.E. degree in applied electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 1991 and 1993, respectively.

In 1993, he joined Nippon Telegraph and Telephone Corporation (NTT), Tokyo. He is now at NTT Lifestyle and Environmental Technology Laboratories, Kanagawa, Japan. He has been engaged in the research and development of low-voltage, low-power SRAM circuits. He is currently doing research on sensing circuits for CMOS fingerprint sensors and developing single-chip fingerprint sensor/identifier LSI's for portable equipment.

Mr. Morimura is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Satoshi Shigematsu (M'93) was born in Tokyo, Japan, on August 2, 1967. He received the B.S. and M.E. degrees in system engineering from Tokyo Denki University, Tokyo, in 1990 and 1992, respectively.

In 1992, he joined Nippon Telegraph and Telephone Corporation (NTT), Tokyo. Since 1992, he has been engaged in the research and development of low-voltage, low-power CMOS circuit. He is now at the NTT Lifestyle and Environmental Technology Laboratories, Kanagawa, Japan. His research interests include biometrics sensor technology and low-power and high-speed circuit design technique. He is currently doing research on parallel processing circuits for CMOS fingerprint identifier and developing single-chip fingerprint sensor and identifier LSI's.

Mr. Shigematsu is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Information Processing Society of Japan.

Katsuyuki Machida (M'99) received the B.S., M.S., and Dr.Eng. degrees in electronics engineering from Kyushu Institute of Technology, Kitakyushu, Japan, in 1979, 1981, and 1995, respectively.

In 1981, he joined the Musashino Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corp. (NTT), Musashino, Tokyo, Japan. Since then, he has been engaged in the development of the interlayer dielectrics process for LSI multilevel interconnection. His current research interests include the advanced functional device fabrication process and sensor for mobile equipment. He is now a Senior Research Engineer and Supervisor at the NTT Telecommunications Energy Laboratories, Atsugi, Kanagawa, Japan. He is an Associate Editor of the *Japanese Journal of Applied Physics*.

Dr. Machida is a member of the Japan Society of Applied Physics.